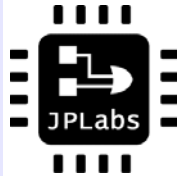


BH1456A

Quadrature Decoder



JPLABS

member of VISIONICS LTD

FEATURES:

- x1 and x4 mode selection
- Up to 32 MHz output clock frequency
- Selectable output mode
- On-chip filtering of inputs for optical or magnetic encoder applications
- Schmitt-Trigger Encoder Inputs
- CMOS & TTL compatible Inputs/Outputs
- From +2.2V to +5V operation (VDD-VSS)

DESCRIPTION:

The BH1456A is an integrated circuit featuring a function of quadrature decoder. A quadrature clock signals derived from optical or magnetic encoders, when applied to the A and B inputs of the BH1456A, are converted to strings of Up Clocks and Down Clocks or to a Clock and an Up/Down direction control signal. These outputs can be interfaced directly with standard Up/Down counters or micro-controllers for direction and position sensing of the encoder.

PINOUT DESCRIPTION:

VDD (Pin 1)

Positive Supply Voltage. From +2.2V to +4V (BH1456AL), +4.5V to +5.5V (BH1456A).

CH A (Pin 2)

Quadrature Clock Input A. This is a Schmitt-Trigger input.

CH B (Pin 3)

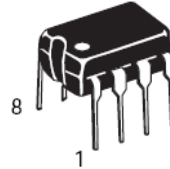
Quadrature Clock Input B. This is a Schmitt-Trigger input.

x4/x1 (Pin 4)

This input selects between x1 and x4 modes of operation. A high-level selects x4 mode and a low-level selects the x1 mode. In x4 mode, an output pulse is generated for every transition at either A or B input. In x1 mode, an output pulse is generated in one combined A/B input cycle.

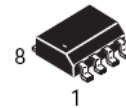
MODE (Pin 5)

This input selects between strings of Up Clocks and Down Clocks or a Clock and an Up/Down direction control signal. A high-level selects the Up Clocks and Down Clocks mode. Low-level



P DIP = PP
PLASTIC PACKAGE
CASE 626

SO 8 = -5P
PLASTIC PACKAGE
CASE 751
(SO-8)



ORDER CODE:

BH1456APP ... P DIP plastic package
BH1456A-5P ... SO-8 plastic package

DIR/CLKDN (Pin 6)

This is the DOWN Clock Output (if MODE is high-level) or Direction Output (if MODE is low-level). This DOWN Clock Output consists of low-going pulses generated when CH A input lags the CH B input. In case of Direction Output (MODE is low-level), the DIR output goes high indicating that the count direction is UP, when CH A input leads the CH B input. When CH A input lags the CH B input, DIR output goes low, indicating that the count direction is DOWN.

CLK/CLKUP (Pin 7)

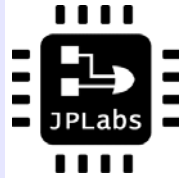
If MODE (pin 5) is low-level, this is the combined UP Clock and DOWN Clock output. The count direction at any instant is indicated by the Direction Output (Pin 6). If MODE (pin 5) is high-level, this is UP Clock output. This output consists of low-going pulses generated when CH A input leads the CH B input.

VSS (Pin 8)

Negative Supply Voltage.

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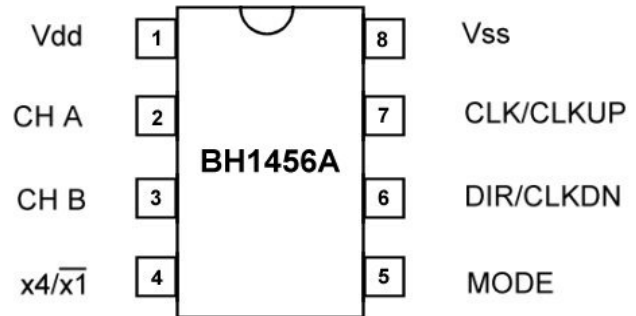


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selects the mode with Clock and an Up/Down direction control signal.

ABSOLUTE MAXIMUM RATINGS:



Ambient temperature	-40°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to Vss, BH1456A	-0.3V to +6.5V
Voltage on VDD with respect to Vss, BH1456AL	-0.3V to +4.0V
Voltage on inputs with respect to Vss	-0.3V to (VDD + 0.3V)
Total power dissipation	800 mW
Maximum current out of Vss pin, -40°C ≤ TA ≤ +85°C	210 mA

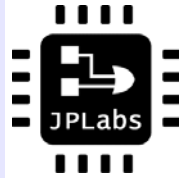
DC ELECTRICAL CHARACTERISTICS:

(All voltages referenced to Vss, TA = 0°C to 70°C.)

PARAMETER	SYMBOL	MIN	MAX	UNITS	CONDITION
Supply voltage	VDD	2.2	5.5	V	
x4/x1 Logic Low	VIL	0.3VDD	-	V	
MODE Logic Low	VIL	0.3VDD	-	V	
A,B Logic Low	VIL	-	0.4	V	VDD = 5V
x4/x1 Logic High	VIH	0.7VDD	-	V	
MODE Logic High	VIH	0.7VDD	-	V	
A,B Logic High	VIH	3	-	V	VDD = 5V
ALL OUTPUTS:					
Sink Current VOL = 0.25V	IOL	15	-	mA	VDD = 5V

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